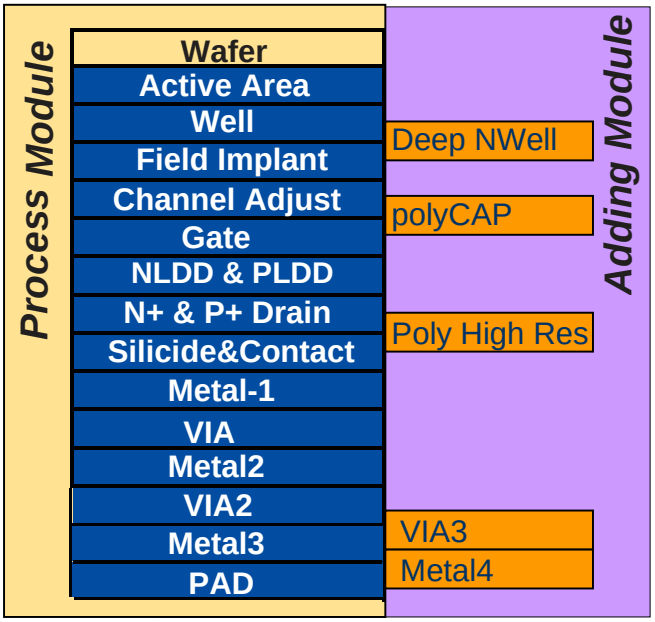
DMS LAB Limited

3.3V&18V 0.35um CMOS process specification

Description

- 3.3V 0.35um CMOS process is DMS Lab Limited Mixed Signal Technology. Main target applications are mixed signal IC's for wide range applications, including automotive, telecommunication and consumer products which using 3.3V supply and 12 or 18V open drain output NMOS transistor.
- Standard element base including 5V NMOS/ PMOS, PNP bipolar and resistors in active can be made by 17 masks core process module.
- Other process modules can be added to integrate HV NMOS transistor (1 mask), PIP capacitors (1 layer), high res polySi-resistors (1 layer), 4-th metal level (2 layers).



Key Features

- 0.35um, triple poly, 4 metal, N-Well process;
- A follow number of different devices are available:

- 3.3V CMOS transistors;
- 3.3V PNP lateral transistors;
- 3.3V PNP vertical transistors;
- 18V NMOS transistors;
- resistors in active layers;
- high res polysilicon resistors;
- PIP and PolySi – gate oxide- Well capacitors;

- BSIM3V3 models for MOS
- Gummel poon models for bipolar;
- CMOS and bipolar cell library;
- Reliable design rules, precise Spice models;

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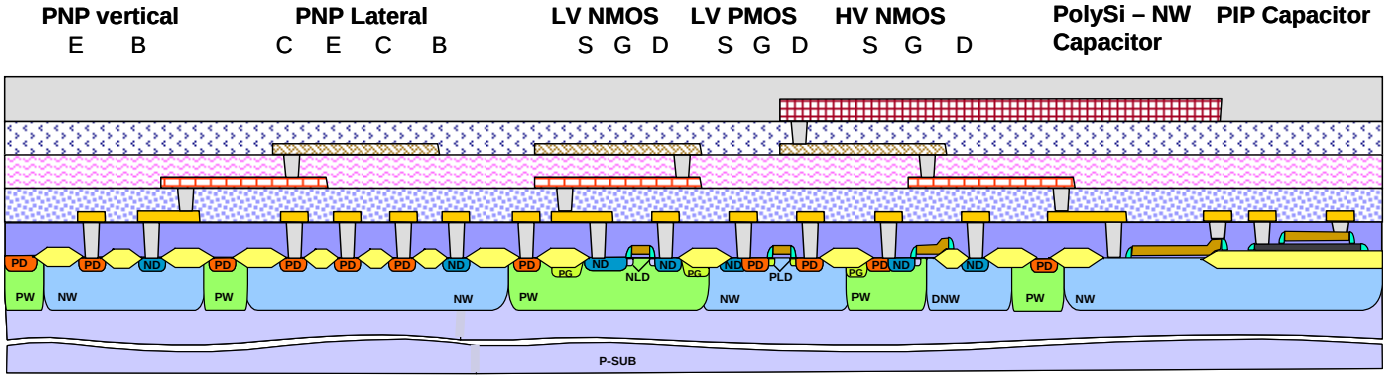
> Schematic cross section of main elements



> Basic design rules

Layer	Min width (um)	Min spacing (um)
Active Area	0.5	0.6
PolySi gate	0.35	0.45
PolySi resistor	0.8	0.6
Contact	0.4	0.5
Metal-1	0.5	0.5
VIA	0.5x0.5	0.45
Metal-2	0.6	0.55
VIA-2	0.5x0.5	0.45
Metal-3	0.6	0.6
VIA-3	0.5x0.5	0.45
Metal-4	0.6	0.6

〉 Device Parameters of main elements

NMOS L=0.35um W=20um

Parameter	Symbol	SPEC			Unit	Measurement condition
		min	type	max		
Threshold voltage	Vth	0.45	0.6	0.75	V	Id=-0.1μA
Drain current	Id	8	10	12.5	mA	Vds=-3.3V, Vg=3.3V
Drain to Source Breakdown Voltage	BVdso	5.0	7.5	-	V	Id=-10μA

PMOS L=0.35um W=20um

Parameter	Symbol	SPEC			Unit	Measurement condition
		min	type	max		
Threshold voltage	Vth	0.55	0.7	0.85	V	Id=-0.1μA
Drain current	Id	3.5	5	6.5	mA	Vds=-3.3V, Vg=3.3V
Drain to Source Breakdown Voltage	BVdso	5	7.5	-	V	Id=-10μA

HV NMOS L=4um (in core process)

Parameter	Symbol	SPEC			Unit	Measurement condition
		min	type	max		
Threshold voltage	Vth	0.45	0.6	0.75	V	Id=-0.1μA
Drain current	Id	75	90	105	uA/um	Vds=-5V, Vg=5V
Drain to Source Breakdown Voltage	BVdso	13	16.5	-	V	Id=-10μA

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HV NMOS L=4um (adding HV module)

Parameter	Symbol	SPEC			Unit	Measurement condition
		min	type	max		
Threshold voltage	Vth	0.65	0.8	0.95	V	Id=-0.1μA
Drain current	Id	155	185	115	uA/um	Vds=-5V, Vg=5V
Drain to Source Breakdown Voltage	BVdso	20	-	-	V	Id=-10μA

VPNP Se=2.4x2.4um^2

Parameter	Symbol	SPEC			Unit	Measurement condition
		min	type	max		
Forward Current Gain	BF	3	4.5	6	-	Vce=-1V, Ib=-10μA
Collector to Emitter Breakdown Voltage	BVceo	7.5	-	-	V	Ic=-10μA

LPNP Se=2.4x2.4um^2

Parameter	Symbol	SPEC			Unit	Measurement condition
		min	type	max		
Forward Current Gain	BF	20	30	45	-	Vce=-1V, Ib=-1μA
Collector to Emitter Breakdown Voltage	BVceo	7.5	-	-	V	Ic=-10μA

RESISTORS

Parameter	Size	SPEC			Unit
		min	type	max	
NDIFF resistor	Wr ≥ 1.0um	65	85	105	Ohm/sq
PDIFF resistor	Wr ≥ 1.0um	110	150	190	Ohm/sq
PolySi resistor (gate)	Wr = 0.6um	30	45	60	Ohm /sq
PolySi resistor (cap)	Wr = 0.6um	75	100	125	Ohm /sq
PolySi high res resistor	Wr = 0.8um	750	1000	1250	Ohm /sq

CAPACITORS

Parameter	SPEC			Unit	Measurement condition
	min	type	max		
PolySi1 – nitride –PolySi2 capacitance	1.35	1.5	1.65	fF/um2	F=1MHz
PolySi2 –gate oxide – Well capacitance	4.0	4.5	5.0	fF/um2	F=1MHz

CONTACT RESISTANCES

Parameter	SPEC			Unit
	min	type	max	
ME1 – NDIFF		2	20	Ohm/contact
ME1 – PDIFF		2	20	Ohm/contact
M1 - PolySi (gate)		2	20	Ohm/contact
M1 - PolySi (cap)		2	20	Ohm/contact
M1 - PolySi (high res)		2	20	Ohm/contact
VIA-1		1.5	6	Ohm/via
VIA-2		1.5	6	Ohm/via
VIA-3		1.5	6	Ohm/via